**BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI-Hyderabad Campus**

**FIRST SEMESTER 2019 - 2020**

**COURSE HANDOUT (PART II)**

Date: 01/ 08 / 2019

In addition to Part I (General Handout for all courses appended to the timetable) this portion gives further specific details regarding the course.

*Course No* : **MEL G624**

*Course Title* : **Advanced VLSI Architecture**

*Instructor-in-charge* : Chetan Kumar V

**1. Scope and Objective:**

The course aims at familiarizing students with advanced parallel processing architectures suitable for high-performance computing. It deals with three levels of parallelism – Instruction-Level, Data Level and Thread Level.

**2. Text Book:**

1. *Computer Architecture: A Quantitative Approach,* by J.L. Hennessy & D.A. Patterson,

Morgan Kaufmann., 5th Ed, 2012.

1. Modern Processor Design: Fundamentals of Superscalar Processors, John Paul Shen & Mikko.H.Lipasti , Tata McGraw Hill,2011.
2. DSP Processor Fundamentals, Phil Lapesly , Jeff Bier, Amit Shoham, Edward.A.Lee, Wiley India Edition,2011.

**3. Reference Books:**

(R1) Parallel Computer Architecture: A Hardware / Software Approach*,* David E Culler &

Jaswinder Pal Singh., Morgan Kauffmann / Harcourt India, 2002.

(R2) Computer Architecture Pipelined& Parallel Processor Design, M.J.Flynn, Narosa Publishing House, 2006

(R3) Advanced Computer Architecture: A Design Space Approach, Sima, Fountain,Kacsuk, Pearson, 2012.

(R3) Journals & Conference Proceedings

**\* It is assumed that students have a working knowledge of MIPS Architecture**

**4. Course Plan:**

|  |  |  |
| --- | --- | --- |
| **No.** | Topics to be covered | **Reference** |
| 1-2 | Fundamentals of Quantitative Design and Analysis | T1- Ch. 1, Class Notes |
| 3-7 | Memory Hierarchy Design | T1- Ch. 2, Class Notes |
| 8 | Introduction to Parallel Processing | T1 – Ch. 3 |
| 9-10 | Introduction to ILP | T1- Ch. 3/ T2-Ch. 1, Class Notes |
| 11-12 | Pipeline architectures | T1- Ch. 3/ T2-Ch. 2, Class Notes |
| 13 | VLIW architectures | T1- Ch. 3, Class Notes |
| 14-16 | Superscalar Architectures | T1- Ch. 3/T2-Ch. 4, 5, Class Notes |
| 17-25 | DSP Architectures | T3, Class Notes |
|  | **Case Studies -1** | Self -Study |
| 26 | Instruction level Data parallel Architecture- Introduction | T1-Ch. 4, Class Notes |
| 27-29 | SIMD Architectures | T1-Ch. 4, Class Notes |
| 30-31 | Vector Processors | T1-Ch. 4, Class Notes |
|  | **Case Studies-2** | Self-Study |
| 32 | Thread & Process Level Parallel Architectures- Introduction | T1-Ch. 5, Class Notes |
| 33-36 | Multi-threaded architectures | T1-Ch. 5, Class Notes |
| 37-39 | Distributed Memory MIMD Architectures | T1-Ch. 5, Class Notes |
| 40-42 | Shared Memory MIMD Architecture | T1-Ch. 5, Class Notes |
|  | Case Studies -3 | Self Study |

The material in the text will be supplemented with papers from Journals. Class Notes will include journal papers, e-material

**5. Evaluation Scheme:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **EC No.** | **Evaluation Component** | Duration **(min)** | Marks (Weightage %) | Date and Time | Nature of Component |
| 1 | Mid-Sem | 90 | 40 (20%) | 30/9 , 09:00 – 10:30 AM | Closed Book |
| 2 | Presentation of Case Studies,  Study Assignments,  Lab based Assignments | …. | 80 (40%) |  | Open Book |
| 3 | Comprehensive | 180 | 80 (40%) | 04/12 FN | Closed Book |

\* Details of the assignments will be announced later.

**6. Chamber Consultation Hours:** *To be Announced*

**7. Make-up Policy:**

Make Up for any component will be given only in genuine cases. In all cases prior intimation must be given to IC.

**9. Notices:** Notices regarding the course will be displayed on moodle.

Instructor - in - charge